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| 09/852,735 | 05/11/2001 | Mototsugu Okushima | NE212-US | 4991 |

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| EXAMINER | |
|---|---|
| KITOV, ZEEV | |
| **ART UNIT** | **PAPER NUMBER** |
| 2836 | |

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/852,735 | OKUSHIMA, MOTOTSUGU | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *37 - 72* is/are pending in the application.

4a) Of the above claim(s) *68 - 72* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37 - 67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Examiner acknowledges submission of the amendment and arguments filed on July 17, 2003. Claims 1 – 36 are deleted; New Claims 37 – 72 are added. Amendment has helped to overcome the objections and rejections under 35 USC paragraph 112. Regarding rejections under 35 USC 102 and 103, the Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

### *Restriction*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 37 - 67, drawn to ESD protection circuit, classified in class 361, subclass 56.

II. Claims 68 - 72, drawn to fabrication method, classified in class 257, subclass 355.

1. Inventions of Group II (Claims 68 – 72) and of Group I (Claims 37 – 67) are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the claimed process can be used for manufacturing of variety of different semiconductor integrated circuits.

2. Newly submitted claims 68- 72 directed to an invention that is independent or distinct from the invention originally claimed for the following reason: unlike Claims 37 – 67 representing the ESD protection circuit, Claims 68 - 72 represent the fabrication method of the ESD protection circuit, which can be used for fabrication of variety of different semiconductor integrated circuits. .

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 68 – 72 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37 - 40, 41, 45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 5,623,387) in a view of Maeda (US 5,471,082). Li et al. disclose most of the elements of the claim including a semiconductor integrated circuit including: a semiconductor substrate (element 301 in Fig. 5B and 5C); a CMOS inner circuit (elements T3 and T4 in Fig. 4A) formed on said semiconductor substrate; and an

ESD protection circuit (elements T121, T124 and Z121, Z124 in Fig.4A), connected between the CMOS inner circuit and a pad, for protecting the CMOS inner circuit against an overvoltage applied to the pad; the ESD protection circuit includes a trigger element (elements Z121, Z124 in Fig. 4A) switching on the bipolar transistor when the overvoltage is applied to said paid. However, it does not disclose a vertical bipolar transistor. Maeda discloses a vertical bipolar transistor (shown in Fig. 38 and 39, col. 14, line 43 – col.15, line 18) designed specifically for ESD protection of semiconductor circuits. The vertical bipolar transistor of Maeda is intended for discharge of an accumulated electric charge of the pad in a direction from a surface of the semiconductor substrate to a depth of the semiconductor substrate. Both references have the same problem solving area, namely providing ESD protection for semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the LI et al. solution by adding the vertical bipolar transistor of Maeda, because as Maeda states (col. 3, lines 7 – 11, 15 – 26), the vertical bipolar transistor has advantage against the lateral bipolar transistor in its ability to conduct excessive currents.

Regarding Claim 38, Maeda discloses the vertical bipolar transistor having such structure that a base and a collector of the transistor are formed in direction from a surface of the semiconductor substrate to a depth (Fig. 33 – 38, col. 14, line 63 – col. 15, line 46), and an emitter of the vertical bipolar transistor is formed on the surface of the semiconductor substrate (col. 15, lines 37 – 46). The motivation for modification of the primary reference is the same as above.

Regarding Claims 39, 40 and 41 Li et al. disclose the trigger element having a diode (element Z 121, Z124 in Fig. 4A) broken down by the overvoltage applied to the pad, and a resistor (elements R121b), which increases a base potential of the vertical bipolar transistor by a trigger current accompanying to a breakdown of the diode. The diode is formed with between a collector and a base of a bipolar transistor having a same structure to that of said vertical bipolar transistor forming the ESD protection circuit (col. 9, line 61 – col.10, line 29), and is broken down by the overvoltage applied to the pad, and a resistor (elements R121b in Fig. 4A) connected between the base and a ground of the bipolar transistor forming the diode, and increases a base potential of the vertical bipolar transistor forming the ESD protection circuit by a trigger current accompanying to a breakdown of the diode.

Regarding Claim 41 Li et al. disclose the diode formed of a reverse diode (element Z121, Z124 in Fig. 4A).

Regarding Claims 45 and 47, Li et al. disclose the trigger element having first and second diodes (elements Z 124 and Z121 in Fig. 4A) and first and second resistors (elements R124b in Fig. 4A), and first and second bipolar transistors of an NPN type (elements T124 and T121 in Fig. 4A); a cathode of said first diode is connected with the pad (element 101 in Fig. 4A) and an anode of the first diode is connected with a base of said first vertical bipolar transistor; a cathode of said second diode is connected with an electric power source terminal (Vcc in Fig. 4A) and an anode of said second diode is connected with a base of the second bipolar transistor; the first resistor (element R124b in Fig. 4A) is connected between the anode of said first diode and a ground terminal;

the second resistor (element R 124b in Fig. 4A) is connected between the anode of the second diode and the pad; a collector of the first vertical bipolar transistor is connected with the pad and an emitter of said first bipolar transistor is connected with the ground terminal; and a collector of the second bipolar transistor is connected with the electric power source terminal and an emitter of the second bipolar transistor is connected with the pad. Both transistors being modified according to Maeda are vertical bipolar transistors. A motivation for modification of primary reference is the same as above.

Claims 42 - 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of Maeda and further in a view of McClure et al. (US 5,774,318). As was stated above Li et al. and Maeda disclose all the elements of Claims 37 and 39. Regarding Claim 42, they do not disclose forward diode. McClure et al. disclose the ESD protection circuit wherein the diode is plural diodes (elements 105 in Fig. 2) and the breakdown (discharge of the ESD charge) occurs due to the diodes conduction. Applying a teaching of McClure et al. to the circuit of Li et al. one of ordinary skill in the art will obtain the Li et al. circuit, wherein two diodes in back biasing direction are replaced by two stacks of diodes connected in forward biasing direction. Both patents have the same problem solving area, namely providing efficient ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the McClure et al. solution of forward biased stack of diodes in the circuit of Li et al., because as McClure et al. state (col. 2, lines 45 – 49), it

will provide flexible way of setting a breakdown voltage by selecting amount of diodes in the stack.

Regarding Claim 43, McClure et al. disclose the forward diode element, which ensures a trigger voltage by connecting in multiple steps. A motivation for modification of the primary reference is the same as above.

Regarding Claim 44, Li et al. disclose the pad as an input terminal. At the same time Li et al. disclose protection against ESD event on power supply terminal (element 121 in Fig. 4A).

Claims 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of Maeda and further in a view of McClure et al. (US 5,774,318). As was stated above, Li et al. and Maeda disclose all elements of Claim 37. However, regarding Claims 49 and 51, they do not disclose two different diodes having a positive bias (i.e. connected by their anode to the pads). McClure et al. disclose the ESD protection circuit wherein the diode is plural diodes (elements 105 in Fig. 2) and the diodes play a role of triggering elements. The resistor is disclosed as an element R3 in Fig. 2. Applying a teaching of McClure et al. to the circuit of Li et al. one of ordinary skill in the art would have modified the Li et al. circuit, to replace two diodes in back biasing direction by two stacks of diodes connected in forward biasing direction. Both patents have the same problem solving area, namely providing efficient ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have used the McClure et al. solution of forward biased stack of diodes in the circuit of Li et al., because as McClure et al. state (col. 2, lines 45 – 49), it will provide flexible way of setting a breakdown voltage by selecting amount of diodes in the stack.

Claims 46, 48, 50, 52 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of Maeda and further in a view of A. Sedra et al. textbook, Microelectronic Circuits. As per Claims 46, 48, 50, 52 and 56, Li et al. discloses an ESD protection circuit that may be modified by the teachings of Maeda as discussed above but none of these references disclose a circuit structure, wherein PNP transistors replace the NPN transistors and the diodes are connected between the base and collector of the transistor in the same polarity. A. Sedra et al. textbook discloses (Fig. 8.9 and 8.10, pp. 408 – 410) that NPN and PNP transistors are functionally equivalent and differ only in their polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Li et al. circuit (T124 and T126 in Fig. 4c) are subject to this conversion. As per diodes positioning, in Fig. 8.10a the diode equivalent element is a battery Vcb, which according to the mirror conversion rules, it is to be transformed into analog of Vbc battery in Fig. 8.10b having the same polarity, i.e. cathodes of both diodes are to be connected to the bases of the transistors, while the anode of the first diode is connected to the ground

terminal and the anode of the second diode is connected to the pad (power supply terminal). The resistors remain positioned according to Li et al., i.e. between the base and the terminal associated with the emitter. The circuit obtained in such transformation is a full equivalent of the original Li et al. circuit and satisfies all the limitations of Claims 46, 48, 50, 52 and 56. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by replacing the NPN transistors by PNP transistors with corresponding changing positions of the diodes according to teaching of Sedra et al., because according to Sedra et al., the NPN and PNP transistors are fully equivalent and mutually replaceable; a choice of particular type of transistors is a routine duty of a designer.

Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of Maeda and further in a view of Shigehara et al. (US 5,539,327) and Kinusaga et al. (5,821,797). As was stated above, Li et al. and Maeda disclose all the elements of Claims 37 and 40. However, regarding Claims 53 and 54, they do not disclose bipolar transistors A – C and resistors connected according to the claim limitations. Shigehara et al. disclose transistors A and C (elements BP1 and N1 in Fig. 6) having their collectors connected to the pad (element 21 in Fig. 6), emitters - to the ground, and their bases connected together and through common resistor Rp1 to the ground. They further disclose transistors B and D (elements BP2 and N2 in Fig. 6) having their collectors connected to the power supply line, their emitters connected to the pad (element 21 in Fig. 6) and their bases connected together and through common

resistor (element Rp2 in Fig. 6) to the ground. Both references have the same problem solving area, namely providing ESED protection to the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by adding the transistors used as diodes in limited avalanche regime according to Shigehara et al., because as Shigehara et al. state (col. 3, line 65 – col. 4, line 2), the breakdown occurs in such circuit at a voltage much lower than the avalanche voltage. As to use of MOSFET transistors N1 and 2 by Shigehera, they can be replaced by bipolar transistors, which would form bipolar transistors C and D. Both references have the same problem solving area, namely providing ESD protection to the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by replacing the MOSFET transistors by the bipolar transistors, since Kinusaga et al. state (col. 4, lines 37 – 46), that the bipolar transistors have substantially higher speed of response.

Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of Maeda, Shigehara et al. and Kinusaga et al. and further in a view of A. Sedra et al. textbook, Microelectronic Circuits. As per Claim 55, they recite a circuit structure of Claim 53, rejected accordingly, wherein PNP transistors replace the NPN transistors and the diodes are connected between the base and collector of the transistor in the same polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a

mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Li et al. circuit (T124 and T126 in Fig. 4c) are subject to this conversion. As per diodes positioning, in Fig. 8.10a the diode equivalent element is a battery Vcb, which according to the mirror conversion rules, it is to be transformed into analog of Vbc battery in Fig. 8.10b having the same polarity, i.e. cathodes of both diodes are to be connected to the bases of the transistors, while the anode of the first diode is connected to the ground terminal and the anode of the second diode is connected to the pad (power supply terminal). The resistors remain positioned according to Li et al., i.e. between the base and the terminal associated with the emitter. The circuit obtained in such transformation is a full equivalent of the original Li et al. circuit and satisfies all the limitations of Claims 55.

Regarding Claims 57 – 67, these claims do not add any identifiable apparatus limitations but merely represent product-by-process claims and therefore are rejected along with the Claim 37, from which they directly or indirectly depend. See discussion bellow in MPEP 2113 [R-1].

**2113 [R-1] Product-by-Process Claims**

PRODUCT-BY-PROCESS CLAIMS ARE NOT LIMITED TO THE MANIPULATIONS OF THE RECITED STEPS, ONLY THE STRUCTURE IMPLIED BY THE STEPS

"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted) (Claim was directed to a novolac color developer. The process of making the developer was allowed. The difference between the inventive process and the prior art was the addition of metal oxide and carboxylic acid as separate ingredients instead of adding the more expensive pre-reacted metal carboxylate. The product-by-process claim was rejected because the end product, in both the prior art and the allowed process, ends up containing metal carboxylate. The fact that the metal carboxylate is not directly added, but is instead produced in-situ does not change the end product.).

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., In re Garnero, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979) (holding "interbonded by interfusion" to limit structure of the claimed composite and noting that terms such as "welded," "intermixed," "ground in place," "press fitted," and "etched" are capable of construction as structural limitations.

### *Respons to Argum nts*

Applicant's Arguments have been carefully considered. However, they are now moot in a view of the new grounds of rejections.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can

be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
03/21/2004

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